Lebanese American University
School of Arts and Sciences
Department of Computer Science and Mathematics

CSC 320 – Computer Organization

Problem Set 2: Computer Abstractions and Technology

Exercise 1

Find the word or phrase from the list below that best matches the description in the following questions. Use the numbers to the left of words in the answer. Each answer should be used only once.

1. virtual worlds	14. operating system
2. desktop computers	15. compiler
3. servers	16. bit
4. low-end servers	17. instruction
5. supercomputers	18. assembly language
6. terabyte	19. machine language
7. petabyte	20. C
8. data centers	21. assembler
9. embedded computers	22. high-level language
10. multicore processors	23. system software
11. VHDL	24. application software
12. RAM	25. Cobol
13. CPU	26. Fortran

1.1 Computer used to run large problems and usually accessed via a network.
Solution: Servers

1.2 10^{15} or 2^{50} bytes
Solution: Petabyte

1.3 A class of computers composed of hundred to thousand processors and terabytes of memory and having the highest performance and cost.
Solution: Super Computers

1.4 Today's science fiction application that probably will be available in the near future
Solution: Virtual Worlds

1.5 A kind of memory called random access memory
Solution: RAM

1.6 Part of a computer called central processor unit
Solution: CPU

1.7 Thousands of processors forming a large cluster
Solution: Datacenters

1.8 Microprocessors containing several processors in the same chip
Solution: Multicore Processors

1.9 Desktop computer without a screen or keyboard usually accessed via a network
Solution: Low-end servers

1.10 A computer used to running one predetermined application or collection of software
Solution: Embedded Computers

1.11 Special language used to describe hardware components
Solution: VHDL

1.12 Personal computer delivering good performance to single users at low cost
Solution: Desktop Computers

1.13 Program that translates statements in high-level language to assembly language
Solution: Compiler

1.14 Program that translates symbolic instructions to binary instructions
Solution: Program that translates symbolic instructions to binary instructions: Assembler

1.15 High-level language for business data processing
Solution: COBOL

1.16 Binary language that the processor can understand
Solution: Machine language

1.17 Commands that the processors understand
Solution: Instruction

1.18 High-level language for scientific computation
Solution: FORTRAN

1.19 Symbolic representation of machine instructions
Solution: Assembly language

1.20 Interface between user's program and hardware providing a variety of services and supervision functions
Solution: Operating systems

1.21 Software/programs developed by the users
Solution: Application Software

1.22 Binary digit (value 0 or 1)
Solution: Bit

1.23 Software layer between the application software and the hardware that includes the operating system and the compilers
Solution: System software

1.24 High-level language used to write application and system software
Solution: C

1.25 Portable language composed of words and algebraic expressions that must be translated into assembly language before run in a compute
Solution: High-level language

1.26 10^{12} or 2^{40} bytes
Solution: Terabyte

Exercise 2

2.1 For a color display using 8 bits for each of the primary colors (red, green, blue) per pixel, what should be a resolution of 1280 x 800 pixels, what should be the size (in bytes) of the frame buffer to store a frame?

Solution:
size of one pixel with three 8-bit colors = $8 \times 3 = 24$ bits/pixel = 3 bytes/pixel
resolution = 1280×800 pixels = 1024000 pixels
size of one frame = 1024000×3 bytes = 3072000 bytes = 2.93 MB

2.2 If a computer has a main memory of 2 GB, how many frames could it store, assuming the memory contains no other information?

Solution:
no. of frames in main memory = 2 GB/2.93MB = 699 frames

2.3 If a computer connected to a 1 gigabit Ethernet network needs to send a 256 Kbytes file, how long it would take?

Solution:
time needed to transfer file = 256 KB/1Gbps = 2.097 ms

2.4 Assuming that a cache memory is ten times faster than a DRAM memory, that DRAM is 100,000 times faster than magnetic disk, and that flash memory is 1000 times faster than disk, find how long it takes to read a file from a DRAM, a disk, and a flash memory if it takes 2 microseconds from the cache memory?

Solution:
time to read from cache = 2 microseconds
time to read from DRAM = time to read from cache × 10 = 20 microseconds
time to read from disk = time to read from DRAM × 100000 = 2 s
time to read from flash memory = time to read from disk /1000 = 2 ms

Exercise 3

Consider three different processors Pl, P2, and P3 executing the same instruction set with the clock rates and CPIs given in the following table.

Processor	Clock Rate	CPI
P1	2 GHz	1.5
P2	1.5 GHz	1.0
P3	3 GHz	2.5

3.1 Which processor has the highest performance?

Solution:
performance = 1/CPU time, where CPU time = instruction count × CPI /clock rate = IC × CPI / clock rate.
performance of P1 = 1/(IC ×1.5/2 GHz) = 1.33×10^9 / IC
performance of P2 = 1/(IC×1/1.5GHz) = 1.5×10^9 / IC

performance of P3 = $1/(IC \times 2.5/3GHz) = 1.2 \times 10^9 / IC$

P2 has the highest performance.

3.2 If the processors each execute a program in 10 seconds, find the number of cycles and the number of instructions.

Solution:

CPU Time of P1=$IC \times 1.5/2GHz=10s$

$\Rightarrow IC = 13.33 \times 10^9$ instructions

$\Rightarrow$no of cycles=$IC \times CPI=13.333 \times 10^9 \times 1.5=20 \times 10^9$ cycles

CPU Time of P2=$IC \times 1/1.5GHz=10s$

$\Rightarrow IC = 15 \times 10^9$ instructions

$\Rightarrow$no of cycles=$IC \times CPI=15 \times 10^9 \times 1=15 \times 10^9$ cycles

CPU Time of P3=$IC \times 2.5/3GHz=10s$

$\Rightarrow IC = 12 \times 10^9$ instructions

$\Rightarrow$no of cycles=$ICxCPI=12x10^9 x2.5=30x10^9$ cycles

3.3 We are trying to reduce the time by 30% but this leads to an increase of 20% in the CPI. What clock rate should we have to get this time reduction?

Solution:

$CPI_{new} = CPI_{old} \times 1.2 \Rightarrow CPI(P1) = 1.8, CPI(P2) = 1.2, CPI(P3) = 3$

clock rate = IC × CPI/CPU time; where new CPU time = $10 \times 0.7 = 7s$

clock rate(P1) = $13.33 \times 10^9 \times 1.8 / 7 = 3.42$ GHz

clock rate(P2) = $15 \times 10^9 \times 1.2 / 7 = 2.57$ GHz

clock rate (P3) = $12 \times 10^9 \times 3 / 7 = 5.14$ GHz

For problems below, use the information in the following table.

Processor	Clock Rate	No. Instructions	Time
P1	2 GHz	20×10^9	7 s
P2	1.5 GHz	30×10^9	10 s
P3	3 GHz	90×10^9	9 s

3.4 Find the IPC (instructions per cycle) for each processor.

Solution:
IPC (P1) = 1/CPI = IC/(CPU time × clock rate) = $20\times10^9/(7\times2\text{GHz}) = 1.428$
IPC (P2) = $30\times10^9/(10\times1.5\text{GHz}) = 2$
IPC (P3) = $90\times10^9/(9\times3\text{GHz}) = 3.33$

3.5 Find the clock rate for P2 that reduces its execution time to that of P1.

Solution:
CPU time_{new}/CPU time_{old} = 7/10 = 0.7
clock rate_{new} = clock rate_{old}/0.7 = 1.5 GHz/0.7 = 2.14 GHz.

3.6 Find the number of instructions for P2 that reduces its execution time to that of P3.

Solution:
CPU time_{new} / CPU time_{old} = 9/10 = 0.9
$IC_{new} = IC_{old} \times 0.9 = 30 \times 10^9 \times 0.9 = 27 \times 10^9$.

Exercise 4

Consider two different implementations of the same instruction set architecture. There are four classes of instructions, A, B, C, and D. The clock rate and CPI of each implementation are given in the following table.

	Clock Rate	**CPI Class A**	**CPI Class B**	**CPI Class C**	**CPI Class D**
P1	1.5 GHz	1	2	3	4
P2	2 GHz	2	2	2	2

4.1 Given a program with 10^6 instructions divided into classes as follows: 10% class A, 20% class B, 50% class C, and 20% class D, which implementation is faster?

Solution:
Class A: 10^5 instr.
Class B: 2×10^5 instr.
Class C: 5×10^5 instr.
Class D: 2×10^5 instr.

CPU time = IC × CPI/clock rate
Total time P1=$(10^5 + 2\times10^5 \times2+5\times10^5 \times3+2\times10^5 \times4)/(1.5\times10^9)$= 1.866 ms
Total time P2=$(10^5 \times2+2\times10^5 \times2+5\times10^5 \times2+2\times10^5\times2)/(2\times10^9)$=1 ms

4.2 What is the global CPI for each implementation?

Solution:
CPI = CPU time × clock rate/IC
CPI (P1) = $1.866 \times 10^{-3} \times 1.5 \times 10^9/10^6 = 2.8$
CPI (P2) = $1 \times 10^{-3} \times 2 \times 10^9/10^6 = 2.0$

4.3 Find the clock cycles required in both cases.

Solution:
clock cycles(P1) = $10^5 \times 1 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 3 + 2 \times 10^5 \times 4 = 28 \times 10^5$
clock cycles(P2) = $10^5 \times 2 + 2 \times 10^5 \times 2 + 5 \times 10^5 \times 2 + 2 \times 10^5 \times 2 = 20 \times 10^5$

The following table shows the number of instructions for a program.

Arith	Store	Load	Branch	Total
500	50	100	50	700

4.4 Assuming that arith instructions take 1 cycle, load and store 5 cycles, and branch 2 cycles, what is the execution time of the program in a 2 GHz processor?

Solution:
$(500 \times 1 + 50 \times 5 + 100 \times 5 + 50 \times 2) / (2 \times 10^9) = 675$ ns

4.5 Find the CPI for the program.

Solution:
CPI = CPU time × clock rate/IC
CPI= $675 \times 10^{-9} \times 2 \times 10^9/700 = 1.928$

4.6 If the number of load instructions can be reduced by one-half, what is the speedup and the CPI?

Solution:
CPU time= $(500 \times 1 + 50 \times 5 + 50 \times 5 + 50 \times 2) / (2 \times 10^9) = 550$ns
Speedup = 675 ns/550 ns = 1.28
CPU time = IC×CPI/clock rate => CPI = $550 \times 10^{-9} \times 2 \times 10^9/650 = 1.69$

Exercise 5

The table below shows the instruction type breakdown of a given application executed on 1, 2, 4, or 8 processors. Using this data, you will be exploring the speed-up of applications on parallel processors.

	Processors	**No. Instructions per Processor**			**CPI**		
		Arithmetic	Load/Store	Branch	Arithmetic	Load/Store	Branch
a.	1	2560	1280	256	1	4	2
	2	1280	640	128	1	4	2
	4	640	320	64	1	4	2
	8	320	160	32	1	4	2

5.1 The table above shows the number of instructions required per processor to complete a program on a multiprocessor with 1, 2, 4, or 8 processors. What is the total number of instructions executed per processor? What is the aggregate number of instructions executed across all processors?

Solution:

Processors	**Instruction per Processor**	**Total instructions**
1	4096	4096
2	2048	4096
4	1024	4096
8	512	4096

5.2 Given the CPI values on the right of the table above, find the total execution time for this program on 1, 2, 4, and 8 processors. Assume that each processor has a 2 GHz clock frequency.

Solution:

Processors	Execution time (ns)
1	4096
2	2048
4	1024
8	512

5.3 If the CPI of the arithmetic instructions was doubled, what would the impact be on the execution time of the program on 1, 2, 4, or 8 processors?

Solution:

Processors	Execution time (ns)
1	5376
2	2688
4	1344
8	672